Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTIONS:**

1. **N. OE**
2. **D0**
3. **D1**
4. **D2**
5. **D3**
6. **D4**
7. **D5**
8. **D6**
9. **D7**
10. **GND**
11. **CP**
12. **Q7**
13. **Q6**
14. **Q5**
15. **Q4**
16. **Q3**
17. **Q2**
18. **Q1**
19. **Q0**
20. **VCC**

**.036”**

**.029”**

**8 7 6 5 4 3**

**2**

**1**

**20**

**19**

**13 14 15 16 17 18**

**9**

**10**

**11**

**12**

**HCT**

**574Y**

**MASK**

**REF**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” X .004”**

**Backside Potential: VCC or FLOATING**

**Mask Ref: HCT574Y**

**APPROVED BY: DK DIE SIZE .029” X .036” DATE: 8/30/21**

**MFG: FAIRCHILD THICKNESS .015” P/N: 54HCT574**

**DG 10.1.2**

#### Rev B, 7/19/02